100MHz
GA-1-C
T_OSC
OUT
U2
74F74
U11
Clock offset
JP11
CKC
CKA
CKB
JP1A
U4
CK1_T
JP3
BT501
DIR
U43
CKEN~
CK50
Enable
T_CL~
16MHz
CK100
JP10
33MHz
TCK
Sync enable
L_CL~
CKA
CKB
CKC
CKC~
U3
CTL = E
LREF = FIF09P
7C421
TFIFO
U10
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BD8
BD(8:0)
Write
T_W~
T_FF~
Clear
T_MR~
Reset
T_RT~
74F273
U9
EF~
TENV
U5
2K2
R4
JP4
ENV_S
VEE
390R
RP7
RP10
U14
U15
TA_D0B
TA_D0A
TA_D1B
TA_D1A
TA_D2B
TA_D2A
TA_D3B
TA_D3A
TA_D4B
TA_D4A
TA_D5B
TA_D5A
TA_D6B
TA_D6A
TA_D7B
TA_D7A
J17 1
J17 2
J17 3
J17 4
J17 5
J17 6
J17 7
J17 8
J17 9
J17 10
J17 11
J17 12
J17 13
J17 14
J17 15
J17 16
R23
1K
U38 10198
Rxt
Cxt
EP
PWC
EN
TR
HS
CK1_I
JP9
CK1_S
CK1_O
ECL hi
R22

NOTE: ON PRODUCTION BOARDS, TEST CIRCUIT COMPONENTS (ALL EXCEPT U41)
ARE OMITTED, AND JUMPERS JP3 AND JP4 ARE SHORTED

PAGE 11	TRIUMF	
DESIGNED BY: A.DAVIEL	787 CCD DATA COMPACTOR MOTHER BOARD	
DRAWN BY: A.DAVIEL		
CHECKED:	TEST DATA GENERATOR	
DATE: APRIL 91		
DWG LIST: DL-1485	DWG NO: B-13326	REV 1